Amendments to the Specification:

Please amend the specification as follows:

Replace the paragraph starting at page 16, line 17 and ending at page 17, the end of line 10 with the following:

FIG. 2 is a sectional view of A-A in the semiconductor apparatus 100 shown in FIG. 1. That is, it is a sectional view of the high withstand voltage NMOS 5. The high withstand voltage NMOS 5 is formed in an area partitioned by the trench 4, out of N type epitaxial layers (low potential reference N type layer 81, high potential reference N type layer 82, and in-NMOS drift layer 85) formed on a P^- type substrate 7. The high withstand voltage NMOS 5 includes gate poly silicon 50*g*, gate oxide film 50*x*, source N^+ region 50*s*, drain N^+ region 50*d*, body P^- region 50*b*, and body contact P^+ region 50*bc*. The gate 50*g*, source 50*s*, and drain 50*d* form a semiconductor transistor that operates in the manner of a relay within the high withstand voltage NMOS 5 region. The NMOS 5 region has formed within it a semiconductor relay device comprising the gate 50*g*, the source 50*s*, and the drain 50*d*. It further includes resurf P^- region 50*r* biased at the same potential (usually 0 V) as the body P^- region 50*b*. Moreover, in-NMOS drift layer 85, field oxide film 9, separation-purpose P^+ diffusion region 10, and others are provided. As shown in FIG. 1, gate wiring 5*g* (not shown in FIG. 2), source wiring 5*s*, and drain wiring 5*d* are provided on the surface of the semiconductor apparatus 100, and the level is shifted by these wirings. An interlayer insulating film 11 is formed between these wirings 5*g*, 5*s*, 5*d* and the N type epitaxial layer. In the high withstand voltage NMOS 5 having such structure, by application of voltage to the gate poly silicon 50*g*, a channel effect is produced in the body P^- region 50*b*, and thereby the conduction between the source N^+ region 50*s* and drain N^+ region 50*d* is controlled.

Replace the paragraph starting at page 17, line 11 and ending at page 18, the end of line 1 with the following:

FIG. 3 is a sectional view of B-B in the semiconductor apparatus 100 shown in FIG. 1. That is, it is a sectional view of the high withstand voltage PMOS 6. The high withstand voltage PMOS 6 is also formed in an area partitioned by the trench 4, out of N type epitaxial layers (low potential reference N type layer 81, high potential reference N type layer 82, and in-PMOS N type layer 86) formed on the P^- type substrate 7. The high withstand voltage PMOS 6 includes gate poly silicon 60*g*, gate oxide film 60*x*, source P^+ region 60*s*, drain P^+ region 60*d*, and sub contact N^+ region 60*sc*. The gate 60*g*, source 60*s*, and drain 60*d* form a semiconductor transistor that operates in the manner of a relay within the high withstand voltage PMOS 6 region. The PMOS 6 region has formed within it a semiconductor relay device comprising the gate 60*g*, the source 60*s*, and the drain 60*d*. It further includes drift P^- region 60*dr* formed in a same diffusion layer as the resurf P^- region 50r in the high withstand voltage NMOS 5. Moreover, same as in the high withstand voltage NMOS 5, field oxide film 9, separation-purpose P^+ diffusion region 10, and others are provided. As shown in FIG. 1, gate wiring 6g (not shown in FIG. 3), source wiring 6s, and drain wiring 6d are provided for shifting the level. In the high withstand voltage PMOS 6 having such structure, by application of voltage to the gate poly silicon 60*g*, a channel effect is produced in the in-PMOS N type layer 86, and thereby the conduction between the source P^+ region 60*s* and drain P^+ region 60*d* is controlled.

Replace the paragraph starting at page 24, line 27 and ending at page 25, the end of line 25 with the following:

FIG. 11 is a sectional view of F-F of the semiconductor apparatus 400 shown in FIG. 10. The semiconductor apparatus 400 of this embodiment has an SOI structure, and includes an embedded insulating layer 75 formed between the P^+ type substrate 7 and epitaxial layers (low potential reference N type layer 81, high potential reference N type layer 82, and separating region N type layer 83). That is, the P^+ type substrate 7 and epitaxial layer are insulated by the embedded insulating layer 75. The substrate positioned beneath the embedded

insulating layer 75 may be either P type or N type. The separating region N type layer 83 is partitioned into plural regions by the trench group 40 the bottom of which reaches the embedded insulating layer 75. Of the regions partitioned by the trench group 40, the region closest to the low potential reference circuit region 1 includes P type diffusion regions 30b, 30bc corresponding respectively to the body P^- region 50b and body contact P^+ region 50bc in the high withstand voltage NMOS 5 (see FIG. 12). The region closest to the high potential reference circuit region 2 includes N type diffusion region 30d corresponding to drain N^+ region 50d in the high withstand voltage NMOS 5. The P type diffusion regions 30b, 30bc are equal in potential to the ground, and the N type diffusion region 30d is equal to the power source of the high potential reference circuit region 2. Potential of the main surface elevates step by step from the low potential reference circuit region 1 toward the high potential reference circuit region 2 by the effect of parasitic ~~capacity~~ capacitance coupling generated by the trench group 40. The coupling ratio of the parasitic ~~capacity~~ capacitance can be adjusted by the width of each trench in the trench group 40 at the stage of design.